second and third pin are selectively connected with a pull down resistor for stabilizing voltage when any of said pins is open.

Please add the following new Claim(s):

Claim 22 (new):

A1

22. A universal testing module according to claim 17 wherein said flip-flop is connected to said second control end.

REMARKS

Claims 1-20, and 22 are now pending. Claims 1-4 and 17-20 are amended. Claim 21 is canceled. Claim 22 is new. No new matter is introduced.

Claims 17-21 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant has amended Claims 17-20, making them dependent from Claim 1, and canceled Claim 21, so as to remove the Examiner's 35 U.S.C. § 112, second paragraph, rejection. Claims 1-4 are also amended to correct a minor grammatical error. No new matter is introduced.

Applicant further respectfully submits Claim 22 is identical to Claim 18, except that said flip-flop is connected to said second control end. Since this configuration was originally recited in Claim 17, no new matter is introduced.

Applicant is also submitting as attached herewith a clean version of the Claims amended.

In the Office Action, the Examiner has indicated that Claims 1-16 are allowed. Applicant respectfully submits that, as discussed above, Claims 17-20 and 22 are now also allowable.

In light of the foregoing, it is believed that the present invention is in condition for allowance. An early and favorable action to that effect is respectfully solicited. If the Examiner has any question, he or she is invited to call or fax Applicant's counsel at the telephone numbers below.

Respectfully Submitted,

01/02/02
Date

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On page 7, lines 12-17:

As shown in FIG. 3, the testing module 10 connects both parallel port 21 and serial port 22 of the computer 20. The logic control unit 11 provides four [pair] pairs of 8-bit input/output ports for transmitting and receiving control or data signals. In other words, there are 4*8=32 input/output lines for controlling and reading signals of all pins of the parallel port 21 and the serial port 22 and detecting the open or short circuit condition. The detailed connection of the pins and ports are shown in FIG. 6.

Claim 1 (once amended):

1. [An] A universal testing module, capable of connecting to a computer having communication ports to be tested and forming communication paths through said ports, for testing the condition of each pin of a parallel port and a serial port of said communication ports, at least comprising:

a logic control unit, having at least a pair of input/output ports for communicating with said parallel port;

a memory unit for storing instructions for controlling said logic control unit and said computer and for temporary exchange of data; and an universal asynchronous receiver/transmitter; and

a voltage converter for voltage interchange of RS-232 and TTL and enabling said logic control unit to communicate with said computer through said serial port and executing said testing.

Claim 2 (once amended):

2. [An] A universal testing module according to claim 1 wherein said memory unit comprises:

an electrically erasable programmable read-only memory for storing machine code instructions for testing said communication port; and

a random-access memory for temporary exchange of data.

Claim 3 (once amended):

3. [An] A universal testing module according to claim 1 wherein said memory unit is located outside said logic control unit.

Claim 4 (once amended):

4. [An] A universal testing module according to claim 1 further comprising a clock circuit for providing time signals, and a reset circuit.

Claim 17 (once amended):

17. A universal testing module according to claim 1 wherein said logic control unit [for testing open condition of a parallel port of a computer, comprising] further comprises:

a first gate having a first data end, a first output end and a first control end;

a second gate having a second data end, a second output end and a second control end;

a flip-flop connecting to either said second control end or said first control end;

a first pin connecting to said first data end;

a second pin connecting to said first control end and said flip-flop;

a third pin connecting to said second data end;

a fourth pin connecting to said first output end and said second output end.

Claim 18 (once amended):

18. A universal testing module [logic control unit] according to claim 17 wherein said flip-flop is [changed to connect] connected to said first control end.

Claim 19 (once amended):

19. A universal testing module [logic control unit] according to claim 17 wherein said first, second and third pin are selectively connected with a pull up resistor for stabilizing voltage when any of said pins is open.

Claim 20 (once amended):

20. A universal testing module [logic control unit] according to claim 17 wherein said first, second and third pin are selectively connected with a pull down resistor for stabilizing voltage when any of said pins is open.